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Transistor mismatch effect on common-mode gain of cross-coupled amplifier

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Abstract

In this paper, the analytical approach of MOS transistor mismatch effect on common-mode gain of cross-coupled amplifier is presented. Transconductance (MOS transistor parameter) mismatch effect on common-mode gain of cross-coupled amplifier was analyzed. This study was started with mathematical derivation for representing the mismatch effect of transconductance between 2 differential pairs of cross-coupled amplifier due to common-mode voltage. The derivation result was simulated based on Monte Carlo simulation with random transconductance mismatch rate from 0.05% until 1%. The common-mode gain increases 36.9 dB and average common-mode gain is -81.1 dB. The transconductance mismatch rate increases followed by increase in common-mode gain. The results can be used by circuit designers to design analog circuits, especially operational amplifier used for biosignals processing to minimize the common-mode gain of their circuits. This research presents aid to circuit designers to improve their circuits performance.

Keywords: *biosignals processing, common-mode gain, cross-coupled amplifier, MOS transistor mismatch, transconductance*

1. Introduction

CMOS cross-coupled amplifier is frequently used in various application. For example, Fully Balanced Differential Difference Amplifier (FBDDA) is mainly constructed by using Cross-Coupled Amplifier (CCA) [1-4]. MOS transistor mismatch often happens after fabrication until 3%, depends on the fabrication technology [5]. There are some MOS transistor parameters which can be considered, such as mismatch in mobility, W/L ratio, oxide capacitance and threshold voltage. Furthermore, the W/L ratio corresponds to transconductance (g_m) [6].

As shown in Figure 1, biosignals, such as Electroencephalogram (EEG), Electrooculogram (EOG), Electrocardiogram (ECG), Electromyogram (EMG) are widely used for medical applications and have small amplitude and low frequency. The biosignals amplitude and frequency are in the order of µV to mV and DC to a few kHz, respectively [7-12]. Common-Mode Rejection Ratio (CMRR) is ratio of differential gain and common-mode gain (A_{cm}). As parameter of CMRR, A_{cm} is important to be reduced when main circuit like CCA is applied for biosignals. The smaller the A_{cm} the better the CMRR [13-15].

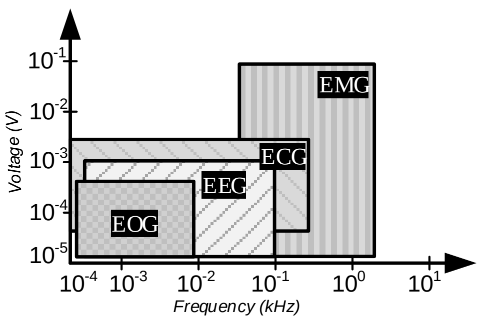

Figure 1. Voltage and frequency ranges of some biosignals

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Furthermore, common-mode voltage (V_{cm}) can be caused by power-line interference which normally has frequency of 50Hz or 60 Hz, depends on local power-line frequency. Therefore, the V_{cm} becomes problem for biosignal processing [16-20]. In this paper, study of g_m mismatch effect on A_{cm} of CCA by large signal analysis (mathematical derivation) and simulation is presented. Section 2 discusses the mathematical derivation of circuit analysis of CCA based on the effect of g_m mismatch on its A_{cm}. Section 3 describes simulation results representing g_m mismatch effect on A_{cm} of CCA. Finally, section 4 concludes this study.

2. Transconductance Mismatch Effect on Cross-coupled Amplifier

In some text books and literatures, CCA can be realized as shown in Figure 2 [2], [21, 22]. It consists of 2 differential pairs which matching between MOS transistors is very important to achieve low common-mode gain. In order to simplified the circuit analysis, R_s and R_d are used with well-matched condition. MOS transistor mismatch often occurs due to W/L ratio which is designed by circuit designer [23]. Furthermore, W/L ratio has relationship with g_m as mentioned in (1) [24, 25]. Therefore, the effect of g_m mismatch on 2 differential pairs of CCA is analyzed in this section.

$$\begin{aligned} g_m &= \frac{\partial I_d}{\partial V_{gs}} \\ &= \sqrt{2\mu C_{ox}\frac{W}{L}|I_d|(1+\lambda V_{ds})} \\ &= \sqrt{2\mu C_{ox}\frac{W}{L}|I_d|} \end{aligned} \tag{1}$$

Firstly, the circuit analysis is started with drain to source current (I_d) definition. Based on large signal analysis, I_d of M_1-M_4 in Figure 1 can be defined as $I_{di} = g_{mi}V_{gsi}|\ i \in \{1,2,3,4\}$. Giving V_{cm} as the input into gates of the MOS transistors, the I_d of the M_1-M_4 become

$$I_{d1,2} = g_{m1,2}(V_{cm} - V_a) \tag{2}$$

$$I_{d3,4} = g_{m3,4}(V_{cm} - V_b) \tag{3}$$

current flows through R_s can be defined as follows:

$$I_{d1} + I_{d2} = \frac{V_a}{R_s} \tag{4}$$

$$I_{d3} + I_{d4} = \frac{V_b}{R_s} \tag{5}$$

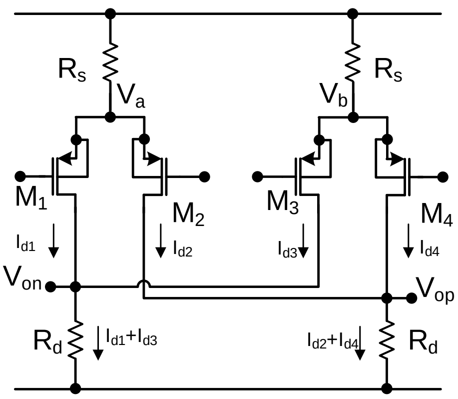

Figure 2. CCA simplified with R_s and R_d

substituting (2–5), V_a and V_b can be derived as follow:

$$V_a = \frac{(g_{m1}+g_{m2})R_s}{(g_{m1}+g_{m2})R_s+1} V_{cm} \tag{6}$$

$$V_b = \frac{(g_{m3}+g_{m4})R_s}{(g_{m3}+g_{m4})R_s+1} V_{cm} \tag{7}$$

on the other hand, V_{op} and V_{on} can be derived as follow:

$$\begin{aligned} V_{op} &= -(I_{d2} + I_{d4})R_d \\ &= -[g_{m2}(V_{cm} - V_a) + g_{m4}(V_{cm} - V_b)]R_d \end{aligned} \tag{8}$$

$$\begin{aligned} V_{on} &= -(I_{d1} + I_{d3})R_d \\ &= -[g_{m1}(V_{cm} - V_a) + g_{m3}(V_{cm} - V_b)]R_d \end{aligned} \tag{9}$$

output voltage (ΔV_{out}) can be calculated as follows:

$$\begin{aligned} \Delta V_{out} &= V_{op} + V_{on} \\ &= [(g_{m1} + g_{m3} - g_{m2} - g_{m4})V_{cm} - (g_{m1} - g_{m2})V_a - (g_{m3} - g_{m4})V_b]R_d \end{aligned} \tag{10}$$

defining ΔV_{cm} as $(V_{cm} + V_{cm})/2$ and mismatched g_{mj} as $g_{mj+1}(1 + \Delta_{j+1})$ | $j \epsilon \{1,3\}$, where Δ_{j+1} is mismatch rate of g_{mj+1}, A_{cm} can be derived as follows.

$$\begin{aligned} A_{cm} &= \frac{\Delta V_{out}}{\Delta V_{cm}} \\ &= \left[g_{m2}\Delta_2 + g_{m4}\Delta_4 - \frac{g_{m2}\Delta_2\alpha R_s}{\alpha R_s+1} - \frac{g_{m4}\Delta_4\beta R_s}{\beta R_s+1}\right] R_d \\ &= \left[g_{m2}\Delta_2\left(1 - \frac{\alpha R_s}{\alpha R_s+1}\right) + g_{m4}\Delta_4\left(\frac{\beta R_s}{\beta R_s+1}\right)\right] R_d \end{aligned} \tag{11}$$

Where α and β stand for $g_{m2}(2 + \Delta_2)$ and $g_{m4}(2 + \Delta_4)$, respectively. From the above derivation, the A_{cm} of CCA is proportional to mismatch of g_m. Based on (11), the A_{cm} is finite, so that some amount of V_{cm} may pass through the CCA. If the CCA is applied to enhanced amplifier, the V_{cm} will be amplified and deteriorate performance of the enhanced amplifier.

3. Simulation Result

In this section, the g_m mismatch effect was evaluated using simulations. Referring to (11), the simulations were done based on the condition on Table 1. Well-matched resistors R_s and R_d were given with the value of 100 kΩ and 2 kΩ, respectively. Mismatch rate of both g_{m1} and g_{m2} are set in the range of 0,05% - 1%.

Table 1. Simulation Condition

Variable	Value
Rs	100 kΩ
Rd	2 kΩ
Δ_2, Δ_4	0,05% - 1%

3.1. Effect of Increasing Mismatch Rate to A_{cm}

In this subsection the effect of increasing Δ is considered and in the next subsection the Δ is extended to random condition. Assuming the Δ of both g_{m1} and g_{m2} increase from 0,05% until 1%. Figure 3 shows simulation result based on the increasing Δ. From the simulation result, the A_{cm} increases from -100 dB until -74 dB. It means the A_{cm} increases 26 dB by the increase of Δ about 1%. This means when Δ is getting bigger, so is the A_{cm}.

3.2. Effect of Random Mismatch Rate to A_{cm}

In order to realize the effect of random mismatch rate, Monte Carlo simulation was used. It was done by 500 times with random and different value of Δ_2 and Δ_4 to get data of A_{cm}. Figure 4 shows histogram of the A_{cm}. Because of random Δ_2 and Δ_4 from 0.05% until 1%, the A_{cm} varies from -111.2 dB to -74.3 dB. From 500 random configuration of Δ_2 and Δ_4 values, most of A_{cm} is in the range from -75 dB to -85 dB, therefore average A_{cm} is -81.1 dB. The random mismatch rate from 0.05% until 1% increases A_{cm} 36.9 dB.

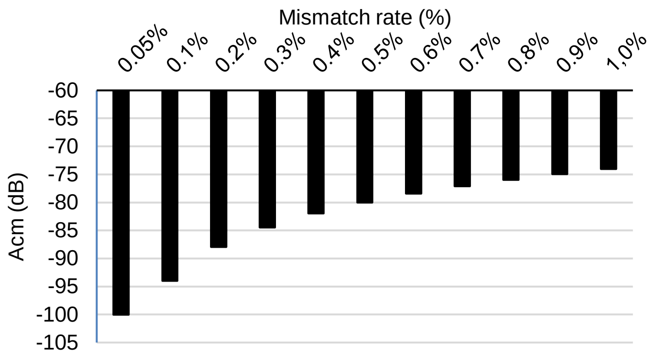

Figure 3. A_{cm} [dB] based on increasing Δ from 0.05% until 1%.

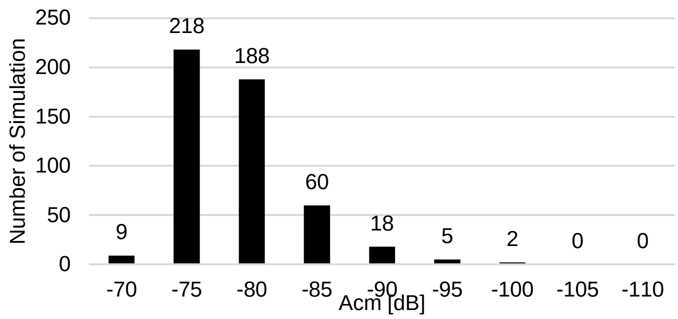

Figure 4. A_{cm} [dB] based on random mismatch rate from 0.05% until 1%.

4. Conclusion

The effect of transistor mismatch on common-mode gain of cross-coupled amplifier has been presented and identified based on mathematical derivation and simulation. The common-mode gain increases along with the increase in transconductance mismatch rate. The results can be used by analog circuit designer to design enhanced operational amplifier with low transistor mismatch effect on common-mode gain.

In the future, mathematical derivation and simulation based on multiple mismatch of MOS transistor parameters such as R_s, R_d, threshold voltage, mobility, and oxide capacitance will be considered in order to represent actual condition. Furthermore, development of common-mode gain reducer and layout technique are also necessary.

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